19. (Amended) A process of manufacturing a multi-layered integrated circuit, comprising:

forming one or more conducting layers;

forming at least one shielding element isolating at least part of said one or more conducting layers;

etching at least said shielding element, thereby forming a surface with both conducting layers and the at least one shielding element;

further processing said one or more conducting layers.

23. (Amended) A method of inhibiting delamination of a cavitation layer in a multi-layered integrated circuit comprising the steps of:

forming a conductive layer;

electrically isolating a first portion of the conductive layer from a second portion thereof with a shielding element;

depositing the cavitation layer over portions of the first portion and the second portion, and over the shielding element; and

etching a trough in the first portion of the conductive layer.

24. (Amended) The method of claim 23, wherein the step of electrically isolating comprises the step of growing a gate oxide layer within a portion of the conductive layer.

25. (Amended) The method of claim 24, further comprising the step of depositing a polycrystalline silicon layer over the gate oxide layer.

Another version of these amended claims, marked up to show all of the changes relative to the previous version of the claims, is filed herewith on pages separate from the amendment, in accordance with 37 CFR § 1.121(c)(1)(ii).

Please add new claims 28-35 as follows:

28. (NEW) The process of Claim 14 wherein the unbroken insulator area is disposed above and within the semiconductor die.

29. (NEW) A process of making a multi-layered integrated circuit, comprising the steps of:

forming, at a surface of a semiconductor die at least an insulating layer;

etching at least said insulating layer thereby forming a surface with a first semiconductor area separated from a second semiconductor area by an unbroken insulating area;

b4 doping the surface, such that said surface includes a first doped semiconductor area in the first semiconductor area electrically isolated from a second doped semiconductor area in the second semiconductor area by the unbroken insulator area.

30. (NEW) The process of Claim 29 wherein the unbroken insulating area extends around the first doped semiconductor area.

31. (NEW) The process of Claim 29, further comprising:

etching a trough in the surface of the first semiconductor area.

32. (NEW) The process of Claim 31, further comprising:

forming a slot in the trough, the slot extending through the semiconductor die.

33. (NEW) A method of inhibiting delamination of a cavitation layer in a multilayered integrated circuit comprising the steps of:

electrically isolating a first conductive portion of a conductive layer from a second conductive portion of the conductive layer with an unbroken shielding element;

depositing the cavitation layer over portions of the first portion and the second portion, and over the shielding element.

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34. (NEW) The method of Claim 33, wherein the unbroken shielding element extends around the first conductive portion of the conductive layer.

35. (NEW) The process of claim 19, further comprising:

doping to increase exposed semiconductor conductance; and

wherein the step of forming at least one shielding element further comprises growing a gate oxide layer, depositing a polycrystalline Silicon layer and etching the gate oxide and polycrystalline Silicon layers using a mask.

REMARKS

In an Office Action mailed November 29, 2002, the Examiner rejected claims 14-20 and 23-27 as being allegedly unpatentable under § 102 and/or § 103. He rejected claims 14-17 as allegedly anticipated by U.S. Patent 5,322,811 (Komuro) under § 102(b), rejected claims 19-20 and 23-27 as allegedly anticipated by U.S. Patent 6,474,780 B1 (Kubota) under § 102(e) and rejected claim 18 as being allegedly unpatentably obvious over Komuro in view of Kubota. The Examiner also rejected Claim 24 under § 112 as being allegedly indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

35 USC § 112

Claim 24 is not indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 24, as amended, recites: